Version with markings to show changes made

In The Title

Please delete the present title and insert therefore the following new title:

MEMORY SHARING ARRANGEMENT FOR AN INTEGRATED MULTIPROCESSOR SYSTEM

In the Claims

17. (New) An electronic product, comprising:

a first processor coupled to an instruction cache and to a data cache;

a first bus coupled to the instruction cache and to the data cache;

a first memory coupled to the first bus;

a second processor coupled to a second bus;

a first bus bridge coupled to the first bus and to the second bus, the first bus bridge providing a path for transferring data between the first memory and the second processor;

a second memory coupled to the first bus;

a second bus bridge coupled to the second bus and a third bus, the third bus providing a data pathway within the first processor, the second bus bridge providing a path for transferring data between the second memory and the third bus of the first processor; and

a direct memory access (DMA) controller coupled to the second bus, the DMA controller configured to manage a transfer of data between the second memory and the second bus bridge;